1. (Previously Presented) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer, said conductive line comprising:

a first portion of said conductive line extending in a first direction, which is parallel to the bit lines, wherein said first portion does not cross said bit lines; and a second portion that extends in a second direction, which is orthogonal to the first direction, and said second portion passes across the bit lines at a plurality of locations. ~~wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step-form having a part extending in the first direction~~.

2-3. (Cancelled)

4. (Original) A semiconductor integrated circuit, according to claim 1, wherein the conductive line has two ends extending toward upper and lower portions of [[a]]the ROM block, respectively.

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Original) A smart card according to claim [[8]]24, wherein

the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

12. (Currently Amended) A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of the component in the ROM; and

a RAM ~~enables~~enabling the CPU to enter and use temporary data during its operation, wherein the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines, wherein

the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

13. (Currently Amended) A smart card according to claim 12~~8~~, wherein the ~~conductive line has~~ two ends both extend~~ing~~ toward the same side of a ROM block.

14. (Cancelled)

15. (Currently Amended) A method for designing a semiconductor integrated circuit according to claim 1, comprising the steps of:

providing bit lines for a ROM extending in a first direction in a first layer;

providing a conductive line arrangement in a second layer, located above the first layer, by an automatic design technique; and

rearranging the conductive line by a manual design technique so that a first portion of said conductive line extends in a first direction, which is parallel to the bit lines, and said first portion does not cross said bit lines; and so a second portion extends in a second direction, which is orthogonal to the first direction, and said second portion passes across the bit lines at a plurality of locations~~conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines~~.

16. (Original) A method according to claim 15, wherein the conductive line is shaped to be a step form having a part extending in the first direction.

17. (Previously Presented) A method according to claim 15, wherein the conductive line is shaped so as to pass across the bit lines two or more times.

18. (Original) A method according to claim 15, wherein

the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

19. (Original) A method according to claim 15, wherein

the conductive line has two ends extending toward a right upper portion and a left lower portion of [[a]]the ROM block, respectively.

20. (Original) A method according to claim 15, wherein

the conductive line has two ends both extending toward the same side of

[[a]]the ROM block.

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Newly Added) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step form having a part extending in the first direction wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

25. (Newly Added) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step form having a part extending in the first direction, wherein the conductive line has two ends both extending toward the same side of a ROM block.

26. (Newly Added) A semiconductor integrated circuit, as recited in claim 4, wherein one of the two ends of the conductive line is arranged adjacent an upper portion of a

side face of the ROM block, and the other of the two ends of the conductive line is arranged at the bottom face of the ROM block, and wherein the side face and the bottom face are orthogonal to one another.